

Sanjana Pillai

Senior Staff Engineer, Physical Design (VLSI)

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PROFILE

Physical-design engineer with 10 years taking SoCs from netlist to tape-out at 16, 7 and 5 nm. Has led timing closure for 9 tape-outs, including a mobile application processor shipping in tens of millions of phones.

PROFESSIONAL EXPERIENCE

- 2020 – Present **Senior Staff Engineer, Physical Design**
Silicore Semiconductors India
- Lead a 12-engineer team for CPU-cluster implementation at 5 nm.
 - Closed timing at 3.2 GHz while cutting dynamic power by 9% with multi-bit flops and clock gating.
 - Built a flow that cut full-chip run time from 30 to 18 hours.
- 2015 – 2020 **Senior Engineer**
Arcwave Systems
- Floorplan, placement and clock-tree synthesis for 4 networking ASICs.
 - Owned IR-drop and EM sign-off for a 600 mm² die.

SELECTED PROJECTS

- 2023 **5 nm mobile CPU cluster**
Silicore Semiconductors
- First-pass silicon success; shipping in phones since 2024.
- 2021 – Present **Open-source PD scripts**
Personal project
- Tcl utilities for timing reports, used by 300+ engineers.

PATENTS

Pillai, S., & Gupta, R. (2023). Method for clock-tree balancing using machine-learned skew prediction. Patent application (filed).

PUBLICATIONS

- Kim, J., Fischer, A., & Pillai, S. (2026). New approaches to RISC-V core verification. *Journal of Low-Power Circuit Design*, 42(4), 577–590.
- Mensah, K., Haddad, N., & Pillai, S. (2026). A study of low-power SRAM design. *Journal of Low-Power Circuit Design*, 23(8), 77–90.
- Rao, S., Pillai, S., Okafor, D., & Kim, J. (2026). Towards analog front-ends for sensors. *Embedded Systems Letters*, 22(12), 180–202.

EDUCATION

- 2013 – 2015 **M.Tech., VLSI Design**
Southern Institute of Technology
CGPA 9.3 / 10
- 2009 – 2013 **B.Tech., Electronics & Communication**
Kerala Coast Engineering College
First Class with Distinction

CERTIFICATIONS

- Advanced physical design certification (EDA vendor)
- Low-power design methodology course (2021)

AWARDS & HONOURS

- Tape-out Excellence Award, Silicore Semiconductors (2023, 2024)
- Best Paper, Asian VLSI Design Conference (2019)

TALKS & PRESENTATIONS

- Keynote: “New approaches to low-power SRAM design”, Semiconductor Test and Reliability, Chennai, 2026.
- Keynote: “Scaling on-chip voltage regulators”, Symposium on Low-Power Circuit Design, Hyderabad, 2026.

TEACHING & TRAINING

- Guest lectures on physical design at 4 engineering colleges

COMMITTEES & COMMUNITY

- Mentor, women-in-semiconductors programme

SKILLS

Physical design: Floorplanning, CTS, routing, STA, IR/EM, physical verification

Tools & scripting: Innovus, ICC2, PrimeTime, Calibre, Tcl, Python

Languages: Malayalam (native), English, Hindi, Telugu

REFERENCES

Available on request.